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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,688	07/13/2001	Yoshinobu Takagi	FUJI 18.846	5601

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EXAMINER	
HO, DUC CHI	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,688	TAKAGI ET AL.	
	Examiner	Art Unit	
	Duc C. Ho	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, and 4-10* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2, 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi et al. (US 5,689,505-in record), hereinafter referred to as Chiussi, in view of Timbs (US 5,878,585-in record) and Lechleider (US 6,359,883), and further in view of Shon (US 5,499,238- IDS record).

Regarding claim 2, Chiussi discloses buffering of multicast cells in switching networks. The ATM is a packet-oriented transfer mode which uses asynchronous time division multiplexing techniques.

an input port part having a plurality of input ports (the input port unit 110-fig. 1 having six input port cards 0-5, see col. 2, lines 37-61);

an output window part having a plurality of buffers (the output port unit 150-fig. 1 having six output port cards 0-5, wherein each card has an ABM (ATM buffer manager) for controlling output buffers sub 0-31, see col. 2, lines 49-51);

a switch part making connections between the plurality of input ports and the plurality of buffers (a switch fabric 130-fig. 1 for connection between the plurality of input ports and the plurality of buffers);

a selection control circuit (the switch fabric 130-fig. 1 has a switch module ASX as a selection control unit) *controlling the switch port so that data from the plurality of input ports are stored in buffers that have available area among the plurality of buffers* (The ASX module-fig. 3 has the circuit 305 and the backpressure 308 for interconnecting input and output ports, see col. 3, lines 23-42) *in accordance with data storage states of the plurality of buffers* (ATM cells received from the input ports are to be processed through stages, see steps 1401-1411, fig .14, and to be stored in the egress queue of the output port card (step 1409). The egress queuing of the output port card uses mechanisms including the egress pointer memory 1012, egress cell memory 1025 of FIG. 10, egress subport bitmaps, and backpressure bitmap for storing the cells in accordance to the available buffers and to the backpressure status of the egress queue at the output port card, see col. 10-line 49 to col. 14-line 10)

Chiussi, however, does not disclose expressly (1) a time division multiplexing part multiplexing the data read from the plurality of buffers in time division multiplexing for

transmission,(2) without detecting a head part of the data, and (3) the plurality of buffers include a plurality of output buffers for each of priority types.

Timbs discloses method and apparatus for converting data streams in a cell based communications system.

Referring to the packet processing unit for processing cells for transmission in figure 10. The processor 701 is provisioned to operate on a synchronous span line multiplexing each channel into and outgoing TDM stream with data reading from buffer 703 to fill the register 702, see col. 12, lines 25-34, and col. 11-line 19 to col. 13-line 14.

One skill in the art would recognize the advantage of using a time division multiplexing part as taught by Timbs into the system of Chiussi so that data read from the buffers would be multiplexed in time division multiplexing for transmission.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Chiussi with Timbs.

The suggestion/motivation for doing so would have been to provide multiplexed data for time division multiplexing for transmission.

Lechleider discloses reducing the variability of the data rates of high-rate data streams in order to communicate such streams over a low-rate channel of fixed capacity. Referring to figure 5, the outputs of input buffers 121, ..., 123 are switched to an array of output buffers 161, ...,164, under the guidance of controller 130, see col. 12, lines 6-53. In other words, data from the plurality of input buffers are caused to be stored into output buffers without employing any information from the header part of the data for such transmission (corresponding to (2)).

One skill in the art would recognize the advantage of using a mechanism for transmission of data as taught by Lechleider into the combination system of Chiussi and Timbs so that data could be read from the inputs to the output buffers, without employing any information from a header part of the data, and to be multiplexed in time division multiplexing for transmission.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Chiussi and Timbs with Lechleider.

The suggestion/motivation for doing so would have been to reduce delay time associated with reading headers of data packets for transmission.

Shon discloses ATM multiplexing process device and method of the broadband integrated service digital network subscriber access apparatus.

The ATM processing device-fig. 2 determines The ATM multiplexing, process device determines whether there is any QOS class buffer 3-fig.2 full (step 20-fig. 5A), and granting the first, second or third priority, etc., to the QOS class buffer 3 in accordance with the principles if not "buffer full", then if there exists any cells in the buffer 3 for each priority, see col. 7, lines 5-45.

One skill in the art would recognize the advantage of using priority at the output buffer as taught by Shon into the combination system of Chiussi, Timbs, and Lechleider so that the output buffers will be used to store data switched from the inputs with different priority types, thereby achieving efficiency in the network for data transmission.

Therefore, it would have been obvious to combine Shon with Chiussi, Timbs, and Lechleider to obtain the invention as specified in claim 2.

Regarding claim 1, the claim has similar limitations as claim 2. Therefore, it is rejected under Chiussi-Timbs-Lechleider-Shon for the same reasons set forth in the rejection of claims 2.

Regarding claim 4, in Lechleider, the indication of a buffer's fullness is equivalent to the claimed limitation "storage states of the plurality of buffer".

Regarding claim 5, in Shon the class buffer part 3-fig. 2 includes a plurality of buffers for each priority types and for data types; and the switch fabric 130-fig.1 of Chiussi (selection control circuit) is capable of causing the different data to be stored in accordance with the states of the buffers for each priority types and data types.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi, Timbs, and Lechleider, in view of Shon, and further in view of Azizoglu et al.(US 6,430,201), hereinafter referred to as Azizoglu.

Regarding claim 10, Chiussi, Timbs, Lechleider, Shon disclose all claimed limitations, except an 8b/10b conversion part the converts multiplexed data from the time division multiplexing part into data having an 8b/10b conversion format for transmission.

Azizoglu discloses method and apparatus for transporting Gigabit Ethernet and fiber channel signals in wavelength-division multiplexed systems. Referring to figure 3 of Azizoglu, a transmitter decodes the 8b/10b encoded GbE/FC signals to reduce their respective signaling rates to no greater than the payload data rate of an OC-48 signal used on the link, see col. 4line 64 to col. 6-line 3.

One skill in the art would recognize the advantage of using a 8b/10b converter as taught by Azizoglu into the system of Chiussi, Timbs, Lechleider and Shon to achieve DC balance and "run length limiting".

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Chiussi, Timbs, Lechleider, and Shon with Azizoglu.

The suggestion/motivation for doing so would have been to achieve DC balance and "run length limiting", i.e., providing a minimum rate of signaling transitions in the data stream to ensure adequate clock recovery at a receiver from the transmission of the time division multiplexed data.

Therefore, it would have been obvious to combine Azizuglo with Chiussi, Timbs, Lechleider, and Shon to obtain the invention as specified in claim 10.

5. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiussi and Timbs, Lechleider, in view of Shon, and further in view of Roy et al. (US 6,646,983-in record), hereinafter referred to as Roy.

Regarding claim 6, Chiussi, Timbs, Lechleider, and Shon disclose all claimed limitations, except the data input to the input port part include an IP packet.

Roy discloses a network switch, which supports TDM, ATM, and variable length packet traffic and include automatic fault/congestion correction. Referring to figure 1, where ATM and IP packets transported in an SPE of the port processor 10-fig. 1, see col. 5, lines 18-46.

One skill in the art would recognize the advantage of having IP packet as the data input to the input ports of the system of Chiussi, Timber, Lechleider, and Shon in order to accommodate different data types and applications that come from sources such as the Internet

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Chiussi, Timbs, Lechleider, Shon and Roy.

The suggestion/motivation for doing so would have been to accommodate different data types and applications that come from sources such as the Internet.

Therefore, it would have been obvious to combine Roy with Chiussi, Timbs, Lechleider, and Shon to obtain the invention as specified in claim 6.

Regarding claim 7, Chiussi, Timbs, Lechleider, and Shon disclose all claimed limitations, except the input port part comprises label add parts, which add labels to the plurality of input ports.

Roy discloses a network switch, which supports TDM, ATM, and variable length packet traffic and include automatic fault/congestion correction. Referring to figure 2B, the switch element 100 includes a JTAG interface 170 for adding tag to data that processed through the input ports.

One skill in the art would recognize the advantage of having a mechanism for tagging data as they are being processed to the input ports of the system of Chiussi, Timber, Lechleider, and Shon in order to distinguish the different data types and applications that are transmitted from different sources including the Internet's applications.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Roy with Chiussi, Timbs, Lechleider, and Shon.

The suggestion/motivation for doing so would have been to distinguish the different data types and applications that are transmitted from different sources including the Internet's applications.

Therefore, it would have been obvious to combine Roy with Chiussi, Timber, Lechleider, and Shon to obtain the invention as specified in claim 7.

Regarding claims 8, and 9, Chiussi, Timbs, Lechleider, and Shon disclose all claimed limitations, except the output port part comprises a SONET frame assembly parts which assemble data read from the plurality of buffers into respective SONET frames, which are then supplied to the time division multiplexing part.

Roy discloses a network switch, which supports TDM, ATM, and variable length packet traffic and include automatic fault/congestion correction. Referring to figure 1, the egress side of the SONET interface includes a SONET framer and TOH generator 40-fig. 1 for assembling SONET input into respective output SONET frames for transmission, see col. 5, lines 18-46.

One skill in the art would recognize the advantage of having a SONET framer for assembling SONET input from the ingress into respective output SONET frames at the egress side and supplied to the Time division multiplexing part for transmission.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Chiussi, Timbs, Lechleider, Shon and Roy.

The suggestion/motivation for doing so would have been to having a SONET framer for assembling SONET input from the ingress into respective output SONET frames at the egress side, and supplying to the TDM multiplexing for transmission.

Therefore, it would have been obvious to combine Roy with Chiussi, Timbs, Lechleider, and Shon to obtain the invention as specified in claims 8-9.

Allowable Subject Matter

6. Claims 11, and 12 are objected to as being independent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc Ho whose telephone number is (571) 272-3147. The examiner can normally be reached on Monday through Friday from 7:00 am to 3:30 pm.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin, can be reached on (571) 272-3134.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2600.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patent Examiner

Duc Ho

04-13-06